



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,724	12/05/2001	William P. Hann	062891.0569 (NUBU 4075)	5117
.5073	7590	02/25/2004	EXAMINER HAN, CLEMENCE S	
BAKER BOTTS L.L.P. 2001 ROSS AVENUE SUITE 600 DALLAS, TX 75201-2980			ART UNIT 2665	PAPER NUMBER

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/008,724	HANN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Clemence Han	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is FINAL.                  2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_ is/are allowed.
- 6) Claim(s) 1-32 is/are rejected.
- 7) Claim(s) \_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All
    - b) Some \*
    - c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)              |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ . | 6) <input type="checkbox"/> Other: ____ .  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. Responsive to amendment received on January 2, 2004, amended claims 9 and 32 are entered as requested.

### ***Claim Rejections - 35 USC § 102***

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
3. Claim 9, 11, 13, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Munter (US Patent 5,475,679).

In regarding to claim 9, Munter teaches the multiplexer 54 receiving data from a first and second channel. Munter also teaches first and second memory banks 58 coupled to the multiplexer. Munter also teaches the scheduler 66, 70 coupled to the memory banks and operable to monitor the first and second memory banks in order to read out cells out of the memory banks (Column 5 Line 52-59).

In regarding to claim 11, Munter teaches a controller 60 determining the location of data storage in the memory 58 (Column 5 Line 37-38).

In regarding to claim 13, Munter teaches a Utopia bus 64 coupled to scheduler 66, 70 and the ATM switch 16.

In regarding to claim 14, Munter teaches a demultiplexer 76 coupled to the ATM switch.

In regarding to claim 15, Munter teaches the dual-port memory 58 coupled to the multiplexer and the scheduler (Column 5 Line 28).

***Claim Rejections - 35 USC § 103***

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claim 1-5, 7, 8, 16-20, 22-28, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Linsley (US Patent 5,583,894) and further in view of Riemann et al. (US Patent 5,892,764).

In regarding to claim 1, 16 and 24, Munter teaches the communicating data from a first channel 50 to a first serial-to-parallel converter 52 and communicating data from a second channel 50 to a second serial-to-parallel converter 52. Munter also teaches the converting the first and second sets of data to a parallel format (Column 5 Line 13-14). Munter also teaches the writing data to memory banks 58. Munter also teaches the scheduler 66, 70 reading cells out of the memory banks 58 to an output communication link 64. Munter, however, does not teach the steps of monitoring the serial-to-parallel converters to determine when one or more words

of data sets have accumulated. Linsley teaches the steps of waiting for word accumulation in serial-to-parallel converter 21 before writing data into the memory 25 (Column 7 Line 24-26). It would have been obvious to one skilled in the art to modify Munter to have the steps of waiting for the word accumulation before writing data into the memory as taught by Linsley in order to use the memory more efficiently. Munter also does not teach the steps of monitoring the memory to determine when enough of the words have formed cells. Riemann teaches the steps of waiting for cell accumulation in the memory (Column 8 Line 64 – Column 9 Line 2). It would have been obvious to one skilled in the art to modify Munter to have the steps of waiting for the cell accumulation before reading the data out to network as taught by Riemann in order to use the network more efficiently.

In regarding to claim 2, 17 and 25, Linsley teaches the steps of generating a memory address (Column 4 Line 55-57).

In regarding to claim 3, 18 and 26, Munter teaches the steps of receiving cells at an ATM switch 16.

In regarding to claim 4, 19 and 27, Munter teaches a scheduler 66, 70 coupled to the memory 58 and a Utopia bus 64.

In regarding to claim 5, 20 and 28, Munter teaches a controller 60 determining the location of data storage in the memory 58 (Column 5 Line 37-38).

In regarding to claim 7, 22 and 30, Munter teaches the steps of storing data in the serial-to-parallel converters 52 into memory 58 via multiplexer 54 under control of select controller 60 (Column 5 Line 14-19).

In regarding to claim 8, 23 and 31, Linsley teaches the steps of incrementing the memory address (Column 4 Line 57-58).

6. Claim 6, 21 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Linsley and Riemann et al. and further in view of Shimada (US 2003/0165147).

In regarding to claim 6, 21 and 29, Munter in view of Linsley and Riemann disclosed the steps of converting serial data to parallel data, storing the accumulated words in the memory and reading out the accumulated cells from the memory. Munter in view of Linsley and Riemann, however, does not teach the steps of sending a write enable signal to the memory. Shimada teaches the steps of sending a write enable signal to the memory [0056]. It would have been obvious to one skilled in the art to include the steps of sending a write enable signal as taught by Shimada to Munter in view of Linsley and Riemann in order to initiate the data transfer to the memory.

7. Claim 10, 12 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munter in view of Hoogenboom (US Patent 6,094,430).

In regarding to claim 10, Munter teaches the multiplexer 54 receiving data from a first and second channel. Munter also teaches first and second memory banks 58 coupled to the multiplexer. Munter also teaches the scheduler 66, 70 coupled to the memory banks and operable to monitor the first and second memory banks in order to read out cells out of the memory banks (Column 5 Line 52-59). Munter, however, does not teach the write controllers operable to communicate words to the multiplexer. Hoogenboom teaches the write controller 360 operable to communicate words to the multiplexer 371-374 (Column 3 Line 35-36). It would have been obvious to one skilled in the art to include the write controller as taught by Hoogenboom to Munter in order to increase the control over memory management.

In regarding to claim 12, Hoogenboom teaches the write controller 360 coupled to multiple serial-to-parallel converters 333-336 to receive data in parallel form (Column 3 Line 29-30).

In regarding to claim 32, Munter teaches the multiplexer 54 receiving data from a first and second channel. Munter also teaches first and second memory banks 58 coupled to the multiplexer. Munter also teaches the scheduler 66, 70 coupled to the memory banks and operable to monitor the first and second memory banks in order to read out cells out of the memory banks (Column 5 Line 52-59).

Munter teaches a controller 60 determining the location of data storage in the memory 58 (Column 5 Line 37-38). Munter, however, does not teach the write controllers to receive parallel data from serial-to-parallel converters. Hoogenboom teaches the write controller 360 coupled to multiple serial-to-parallel converters 333-336 to receive data in parallel form (Column 3 Line 29-30). It would have been obvious to one skilled in the art to include the write controller as taught by Hoogenboom to Munter in order to increase the control over memory management.

***Response to Arguments***

8. Applicant's arguments filed on January 2, 2004 have been fully considered but they are not persuasive.
9. In regarding to claim 9 and 32, the applicants argue that Munter fails to teach, suggest or disclose a scheduler coupled to each of the first and second memory banks and operable to monitor the first and second memory banks in order to read one or more cells out of a selected one of the first and second memory banks. The applicants further argue that the examiner concedes "Munter also does not teach the steps of monitoring the memory to determine when enough of the words have formed cells" (Applicants remark Page 10). First of all, the steps of "to monitor the first and second memory banks" is newly added in the amended claim 9 and 32. Second, the steps of "monitoring memory to read cells out of a selected memory" is different limitation from the steps of "monitoring memory to determine when enough of the words have formed cells". After all, Munter teaches the steps of "monitoring memory to read cells out of a selected memory" (Column 5 Line 52-59).

Therefore, the examiner contends that Munter teaches scheduler 66, 70 coupled to each of the first and second memory banks 58 and operable to monitor

the first and second memory banks in order to read one or more cells out of a selected one of the first and second memory banks (Column 5 Line 52-59).

10. In regarding to claim 1, the applicants argue that neither Munter nor Linsley teaches “the monitoring operations” (Applicants remark Page 12-13). Claim 1 is rejected as being unpatentable over Munter in view of Linsley and further in view of Riemann et al.. There are two monitoring operations in claim 1. The first one is monitoring the serial-to-parallel converter for the data accumulation. Linsley teaches the steps of waiting for word accumulation in serial-to-parallel converter 21 before writing data into the memory 25 (Column 7 Line 24-26). The second one is monitoring the scheduler for the data accumulation. Riemann teaches the steps of waiting for cell accumulation in the memory (Column 8 Line 64 – Column 9 Line 2).

Therefore, the examiner contends that Munter in view of Linsley and further in view of Riemann et al. teaches the monitoring operations.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (703) 305-0372. The examiner can normally be reached on Monday-Friday 8 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Han  
Clemence Han  
Examiner  
Art Unit 2665



HUY D. VU  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600